IN THE CLAIMS

Please cancel claims 2 and 5-9 without prejudice, amend claims 1, 3-4 and 10, and add claims 11-21 as follows:

1. (Currently amended) A rate matching circuit for adjusting the number of bits in a data block, the data block comprising a plurality of interleaved words generated by the action of an interleaving circuit on a coded output generated by the action of a coding circuit on a digital input, the coded output having a greater number of bits than the digital input, the rate matching circuit having means for adjusting the number of bits in the data block using a rate matching pattern to provide data bits for transmission during respective frames of a transmission channel, ~~characterised in that~~ and means ~~are provided~~ for selecting the rate matching pattern depending on ~~the characteristics of the coding circuit and of the interleaving circuit~~ a bit deletion/repetition rate, wherein a bit deletion/repetition pattern is selected to ensure that the deleted or repeated bits are not required to enable all bits from the digital input to be reconstructed.

2. (Canceled)

3.(Currently amended) A rate matching circuit as claimed in claim 1 ~~or 2, characterised in that~~ , wherein the rate matching pattern for each interleaved word within the data block is offset with respect to the adjacent interleaved word or words within the block.

4.(Currently amended) A rate matching circuit as claimed in ~~any one of~~ claims ~~1 to 3, characterised in that~~ , wherein the rate matching pattern is selected as a function of the interleaving depth of the interleaving circuit.

Claims 5-9. (Canceled)

10.(Currently amended) A method of operating a rate matching circuit to adjust the number of bits in a data block, the data block comprising a plurality of interleaved words generated by the action of an interleaving circuit on a coded output generated by the action of a coding circuit on a digital input, the coded output having a greater number of bits than the digital input, the rate matching circuit adjusting the number of bits in the data block using a rate matching pattern to provide data bits for transmission

during respective frames of a transmission channel, ~~characterised by~~ and selecting the rate matching pattern depending on ~~the characteristics of the coding circuit and of the interleaving circuit~~ a bit deletion/repetition rate, wherein a bit deletion/repetition pattern is selected to ensure that the deleted or repeated bits are not required to enable all bits from the digital input to be reconstructed.

11. (New) The rate matching circuit of claim 1, wherein the rate matching pattern forms a matrix including change bits that indicate change of corresponding bits of said interleaved words within said data block, wherein each row of said matrix includes a maximum of one of said change bits.

12. (New) The rate matching circuit of claim 1, wherein said coding circuit has one of a fixed code rate and a predetermined number of rates for a variable data source.

13. (New) The rate matching circuit of claim 1, wherein said interleaving circuit is not adaptive.

14. (New) The rate matching circuit of claim 1, wherein said interleaving circuit has a constant bit rate.

15. (New) The rate matching circuit of claim 1, wherein said coding circuit has one of a fixed code rate and a predetermined number of rates for a variable data source, and wherein said interleaving circuit is not adaptive.

16. (New) The rate matching circuit of claim 1, wherein said rate matching circuit alters a coding rate of said coding circuit.

17. (New) The method of claim 10, wherein change bits of said rate matching pattern for deleting or repeating bits of said data block are offset with respect to the each other.

18. (New) The method of claim 10, wherein change bits of said rate matching pattern for deleting or repeating bits of said data block are offset with respect to the each other along adjacent columns of a matrix of said rate matching pattern.

19. (New) The method of claim 10, wherein change bits of said rate matching pattern for deleting or repeating bits of said data

block are offset with respect to the each other along adjacent rows of a matrix of said rate matching pattern.

20. (New) The method of claim 10, wherein change bits of said rate matching pattern for deleting or repeating bits of said data block are offset with respect to the each other along adjacent rows and columns of said rate matching pattern.

21. (New) The method of claim 10, wherein said interleaving circuit forms said data block by filling a matrix row by row with row bits of said coded output and outputs column bits of said matrix column by column to form said interleaved words.